KARTA OPISU MODUŁU KSZTAŁCENIA

Nazwa modułu/przedmiotu			Kod
Testing of Digital Systems			**1010802131010812917**
Kierunek studiów	Profil kształcenia (ogólnoakademicki, praktyczny)	Rok / Semestr	
Electronics and Telecommunications	**ogólnoakademicki**	**2 / 3**	
Ścieżka obieralności/specjalność	Przedmiot oferowany w języku:	Kurs (obligatoryjny/obieralny)	
Information and Communication	**angielski**	**obieralny**	

Stopień studiów:	Forma studiów (stacjonarna/niestacjonarna)
II stopień	**stacjonarna**

Godziny				Liczba punktów
Wykłady: **2**	Ćwiczenia: **-**	Laboratoria: **1**	Projekty/seminaria: **-**	**3**

Status przedmiotu w programie studiów (podstawowy, kierunkowy, inny)	(ogólnouczelniany, z innego kierunku)
kierunkowy	**z danego kierunku**

Obszar(y) kształcenia i dziedzina(y) nauki i sztuki	Podział ECTS (liczba i %)
nauki techniczne	**3 100%**
nauki techniczne	**3 100%**

Odpowiedzialny za przedmiot / wykładowca:

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Wymagania wstępne w zakresie wiedzy, umiejętności, kompetencji społecznych:

1	**Wiedza:**	Knows how to analyze and synthesize digital circuits and systems. Knows basic computer-aided design (CAD) tools used in synthesis and test of digital circuits.
2	**Umiejętności:**	Can design a digital circuit taking into account various criteria and by deploying adequate methods and tools. Can use standard libraries, catalog data, application notes, and CAD tools for handling semiconductor circuits and systems.
3	**Kompetencje społeczne**	Demonstrates responsibility for designed electronic circuits and systems. Is aware of the hazards they pose for individuals and communities if they are improperly designed or produced.

Cel przedmiotu:

This course provides a comprehensive coverage of state-of-the-art digital circuit testing techniques, including practices and automation tools for high-quality low-cost manufacturing test. In addition to fault modeling, test generation and fault simulation, it covers design for testability, built-in self-test for random logic and memory arrays altogether with the newest topics related to embedded test methodologies developed specifically to reduce test data volume, test time, and yield learning.

Efekty kształcenia i odniesienie do kierunkowych efektów kształcenia

Wiedza:

1. A thorough understanding of problems related to fault detection and diagnosis in VLSI combinational and sequential digital circuits, including usage of automated tools for test generation, fault simulation, design for testability, and built-in self-test. - [K1_W12]

2. Basic fault models, can assess their impact on complexity of both test generation and fault simulation. They are also able to choose an adequate method for test data compression and memory test. - [K1_W12]

3. Basics of test economy and relationships between quality of test and reliability of VLSI semiconductor circuits. They can assess the cost of test given a test technology, automated test equipment, timing constraints, and test objectives. - [K1_W12]

Umiejętności:

1. A student can use commercial computer-aided design (CAD) tools to run test pattern generation, fault simulation, scan insertion, and several other tasks related to either testing or designing easy to test digital circuits. - [K1_U16]

2. Using commercial CAD tolls, a student can design a circuit with various test features, including scan chains, test points, on-chip test pattern generators, and test response compactors. - [K1_U16]

3. A student can critically analyze methods proposed to perform fault detection and diagnosis in complex digital designs, including their impact on hardware complexity of test logic, the resultant performance of the circuit and its power budget in the test mode. - [K1_U16]

Kompetencje społeczne:

1. Appreciate the practical significance of the systems developed in the course. - [K1_K01]

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Sposoby sprawdzenia efektów kształcenia

A written final exam is given during the end-of-term exam week. This is followed by considerable discussion among the teaching staff to factor in diligence on the homework and labs, and participation in classes and tutorials. This discussion can affect a final grade for the course.

Treści programowe

This course reviews the most essential and timely issues related to various aspects of testing of microelectronics digital circuits. It is composed of a representative sample of the state of the art solutions in the following areas: economics of test, fault modeling, test pattern generation, fault simulation, design for testability, built-in self-test, fault diagnosis, semiconductor memory test, system-level test, embedded test for high-quality low-cost manufacturing, automation tools and design flows. Special emphasis is placed on issues related to test compression and at-speed testing. All lectures are illustrated with various applications and case studies.

Literatura podstawowa:

1. M. Abramovici, M.A. Breuer, A.D. Friedman, Digital systems testing and testable design, IEEE Press, New York 1995.
2. L.-T. Wang, C.-W. Wu, X. Wen, VLSI test principles and architectures, Elsevier, Amsterdam 2006.
3. H. Jha, S. Gupta, Testing of digital systems, Cambridge University Press, Cambridge 2003.
4. J. Rajski, J. Tyszer, Arithmetic built-in self-test, Prentice Hall, Upper Sadle River 1998.
5. M.L. Bushnell, V.D. Agrawal, Essentials of electronic testing, Kluwer Academic Publishers, Boston 2000.

Literatura uzupełniająca:

1. L.-T. Wang, C.-W. Wu, X. Wen, VLSI test principles and architectures, Elsevier, Boston 2006.

Bilans nakładu pracy przeciętnego studenta

Czynność	Czas (godz.)
1. Wykład	30
2. Udział w ćwiczeniach laboratoryjnych	15
3. Wykonywanie mini-projektów zespołowo lub indywidualne	10
4. Praca własna	10
5. Przygotowanie się do egzaminu	10
6. Konsultacje z wykładowcami	3
7. Udział w egzaminie	2

Obciążenie pracą studenta

forma aktywności	godzin	ECTS
Łączny nakład pracy	80	3
Zajęcia wymagające bezpośredniego kontaktu z nauczycielem	50	2
Zajęcia o charakterze praktycznym	25	1